WHAT IS CLAIMED IS:

1. A semiconductor device, comprising multiple through electrodes in a semiconductor chip linking a front surface to a back surface thereof,

wherein

the through electrodes have mutually differing cross-sectional areas.

2. The semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is contact through electrodes electrically connected to the semiconductor chip.

3. The semiconductor device as set forth in claim 1, wherein at least one type of the through electrodes is non-contact through electrodes not electrically connected to the semiconductor chip.

4. The semiconductor device as set forth in claim 2, wherein at least one type of the through electrodes is non-contact through electrodes not electrically connected to the semiconductor chip.

5. The semiconductor device as set forth in claim 1,

wherein the cross-sectional areas are increased according to a magnitude of an electric current via the through electrodes.

6. The semiconductor device as set forth in claim 2, wherein the cross-sectional areas are increased according to a magnitude of an electric current via the through electrodes.

7. The semiconductor device as set forth in claim 3, wherein the cross-sectional areas are increased according to a magnitude of an electric current via the through electrodes.

8. The semiconductor device as set forth in claim 4, wherein the cross-sectional areas are increased according to a magnitude of an electric current via the through electrodes.

9. The semiconductor device as set forth in claim 1, wherein the cross-sectional areas of those through electrodes which are connected to a ground terminal or a power supply terminal of the semiconductor chip are greater than the cross-sectional areas of those through electrodes which are connected to a signal terminal.

10. The semiconductor device as set forth in claim 2, wherein the cross-sectional areas of those through electrodes which are connected to a ground terminal or a power supply terminal of the semiconductor chip are greater than the cross-sectional areas of those through electrodes which are connected to a signal terminal.

11. The semiconductor device as set forth in claim 3, wherein the cross-sectional areas of those through electrodes which are connected to a ground terminal or a power supply terminal of the semiconductor chip are greater than the cross-sectional areas of those through electrodes which are connected to a signal terminal.

12. The semiconductor device as set forth in claim 4, wherein the cross-sectional areas of those through electrodes which are connected to a ground terminal or a power supply terminal of the semiconductor chip are greater than the cross-sectional areas of those through electrodes which are connected to a signal terminal.

13. A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including multiple through electrodes therein linking

a front surface to a back surface thereof,

wherein

the through electrodes have mutually differing cross-sectional areas.

14. A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including multiple through electrodes therein linking a front surface to a back surface thereof,

wherein:

the through electrodes have mutually differing cross-sectional areas; and

at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip.

15. A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including multiple through electrodes therein linking a front surface to a back surface thereof,

wherein:

the through electrodes have mutually differing cross-sectional areas; and

at least one type of the through electrodes is non-contact through electrodes not electrically connected

to that semiconductor chip.

16. A chip-stack semiconductor device, comprising multiple stacked semiconductor chips, each of the semiconductor chips including multiple through electrodes therein linking a front surface to a back surface thereof,

wherein:

the through electrodes have mutually differing cross-sectional areas;

at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip; and

at least one type of the through electrodes is non-contact through electrodes not electrically connected to that semiconductor chip.

17. The chip-stack semiconductor device as set forth in claim 13, wherein the cross-sectional areas of those through electrodes which connect n+1 or more adjacent semiconductor chips are greater than the cross-sectional areas of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

18. The chip-stack semiconductor device as set forth in

claim 14, wherein the cross-sectional areas of those through electrodes which connect n+1 or more adjacent semiconductor chips are greater than the cross-sectional areas of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

19. The chip-stack semiconductor device as set forth in claim 15, wherein the cross-sectional areas of those through electrodes which connect n+1 or more adjacent semiconductor chips are greater than the cross-sectional areas of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

20. The chip-stack semiconductor device as set forth in claim 16, wherein the cross-sectional areas of those through electrodes which connect n+1 or more adjacent semiconductor chips are greater than the cross-sectional areas of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2.

21. The chip-stack semiconductor device as set forth in claim 13, wherein the cross-sectional areas are increased

according to an interconnect line length through the multiple stacked semiconductor chips.

22. The chip-stack semiconductor device as set forth in claim 14, wherein the cross-sectional areas are increased according to an interconnect line length through the multiple stacked semiconductor chips.

23. The chip-stack semiconductor device as set forth in claim 15, wherein the cross-sectional areas are increased according to an interconnect line length through the multiple stacked semiconductor chips.

24. The chip-stack semiconductor device as set forth in claim 16, wherein the cross-sectional areas are increased according to an interconnect line length through the multiple stacked semiconductor chips.

25. The chip-stack semiconductor device as set forth in claim 21, wherein the cross-sectional areas are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

26. The chip-stack semiconductor device as set forth in claim 22, wherein the cross-sectional areas are increased

in proportion to an interconnect line length through the multiple stacked semiconductor chips.

27. The chip-stack semiconductor device as set forth in claim 23, wherein the cross-sectional areas are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.

28. The chip-stack semiconductor device as set forth in claim 24, wherein the cross-sectional areas are increased in proportion to an interconnect line length through the multiple stacked semiconductor chips.